## IN THE CLAIMS

Please amend the claims as follows:

1-45. (Canceled)

46. (Previously Presented) A memory, comprising:

a memory array;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array; and

wherein the memory array, control circuit and I/O circuit each comprise:

a layer of a titanium alloy, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.

47. (Original) The memory of claim 46, wherein the titanium alloy comprises titanium and zinc.

48-56. (Canceled)

57. (Currently Amended) A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises

a layer of a titanium alloy formed overlying walls of a contact hole, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.

58. (Currently Amended) A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; ~~and~~

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises a via having

a layer of a titanium alloy formed overlying walls of a contact hole, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer; and

a fill coupled to the titanium alloy layer, wherein the fill comprises a metal selected from the group consisting of tungsten and aluminum.

59. (Currently Amended) A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises

a layer of a titanium alloy formed overlying walls of a contact hole, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer;

wherein the titanium alloy layer is produced using a method, the method comprising:

forming a seed layer within the contact opening by combining a first precursor with a first reducing agent; and

forming the titanium alloy layer within the contact opening by combining a titanium-containing precursor with the seed layer.

60. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

61. (Previously Presented) The memory device of claim 60, wherein the titanium alloy includes titanium and zinc.

62. (Previously Presented) The memory device of claim 60, wherein the insulator layer includes silicon dioxide ($SiO_2$).

63. (Previously Presented) The memory device of claim 60, wherein the electronic device includes a transistor.

64. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

65. (Previously Presented) The memory device of claim 64, wherein the titanium alloy includes titanium and zinc.

66. (Previously Presented) The memory device of claim 64, wherein the insulator layer includes silicon dioxide ($SiO_2$).

67. (Previously Presented) The memory device of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

68. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphosilicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the borophosphosilicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

69. (Previously Presented) The memory device of claim 68, wherein the titanium alloy includes titanium and zinc.

70. (Previously Presented) The memory device of claim 68, wherein the electronic device includes a transistor.

71. (Previously Presented) The memory device of claim 68, wherein the contact opening includes a high aspect ratio contact opening.

72. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active

region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

73. (Previously Presented) The memory device of claim 72, wherein the titanium alloy includes titanium and zinc.

74. (Previously Presented) The memory device of claim 72, wherein the electronic device includes a transistor.

75. (Previously Presented) The memory device of claim 72, wherein the insulator layer includes silicon dioxide ($SiO_2$).

76. (Previously Presented) The memory device of claim 72, wherein the insulator layer includes borophosphosilicate glass (BPSG).

77. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from

the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

78. (Previously Presented) The memory device of claim 77, wherein the titanium alloy includes titanium and zinc.

79. (Previously Presented) The memory device of claim 77, wherein the insulator layer includes silicon dioxide ($SiO_2$).

80. (Previously Presented) The memory device of claim 77, wherein the insulator layer includes borophosphosilicate glass (BPSG).

81. (Previously Presented) A memory device, comprising:

a semiconductor substrate;

a memory array coupled to the semiconductor substrate;

a control circuit, operatively coupled to the memory array;

an I/O circuit, operatively coupled to the memory array;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphosilicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphosilicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the alloy layer.

82. (Previously Presented) The memory device of claim 81, wherein the titanium alloy includes titanium and zinc.

83. (New) A memory device, comprising:

a memory array;

a control circuit operatively coupled to the memory array; and

an I/O circuit operatively coupled to the memory array;

wherein at least one of the memory array, control circuit and I/O circuit comprises

a layer of a titanium alloy formed by chemical vapor deposition at a temperature range of 300 to 550 degrees Centigrade at a gas pressure range of 0.1 torr to 10 torr, and overlying walls of a contact hole with a step coverage of more than 90%; and

a titanium silicide contact having a composition that is different from the layer of titanium alloy, the contact being directly coupled to the layer.

84. (New) The memory device of claim 83, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony.